REMARKS

Claim 25, 28-29 and 33 have been amended. Accordingly, claims 25-34 are currently pending.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority.

Information Disclosure

Applicants appreciate the return of the PTO-1449 form filed on December 9, 2003. However, the citation of US Patent No. 6,469,948 was not initialed. Accordingly, Applicants resubmit the PTO-1449 form and request acknowledgement that the document has been considered by initialing the citation and returning the form.

35 U.S.C. §102

Claims 25-27 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Wu et al. U.S. Patent No. 6,329,997. Applicants request reconsideration of the rejection for the following reasons.

The Office Action relies upon Wu for disclosing a (3-D graphics) chip 40 as shown in Fig. 2 having first and second access ports (FIFOs 46-54) and memory banks 62, 64 and 66, as shown in Fig. 3. Priority of the first and second access ports when accessing the same memory bank is determined by an access priority engine 56 as seen in Fig. 2. However, the access priority engine 56 in Wu allows only one FIFO to access the memory at a time. This is described in Wu at col. 5, lines 6-11, as follows.

> "The purpose of the access priority engine 56 is to determine which FIFO's are [to] requesting access to the embedded DRAM buffers via the wide access bandwidth bus 58, and to grant access to each requesting FIFO, one-at-a-time, such that...."

The access priority engine in Wu, therefore, is for the arbitration of the memory access and the access priority engine allows only one port to access the memory at a time.

In another embodiment shown in Fig. 3, a texture buffer (embedded bank 1) and Z-buffer (embedded bank 2) has individual access buses 78 and 80, respectively. Each access bus has its own access priority engine (56 Of Fig. 2). This is described in col. 5 of Wu, lines 56-60. In another embodiment shown in Fig. 4 of Wu, the texture buffer and the

Z-buffer reside within a single embedded DRAM (col. 6, lines 24-25). In this embodiment, the priority access engine serves the same function as described above (col. 6, lines 39-40). Wu comments that as a result: "The effective drawing process throughput in the specific embodiment illustrated in Fig. 4 is not as high as the throughput for the embodiment illustrated in Fig. 3." (col. 6, lines 42-44). This is because, in the embodiment of Fig. 4, the two 3-D drawing engines compete for access to their respective drawing buffers and lower throughput results (col. 6, lines 55-56).

In still another embodiment shown in Fig. 5 of Wu, programmable switches 122 are employed. The switches are programmable by a host device (col. 7, lines 19-20). This means the access provided by the switches 122 is not the result of the function of the priority engine, but rather as a result of programming by the host. One having ordinary skill in the art would realize that this configuration is feasible only when the relationship between the accessor and memory is one to one, is known in advance, and does not change dynamically during the operation.

On the other hand, in the present invention, the access priority judgment unit allows two accesses in parallel so long as different banks are accessed. See page 30 of the specification, lines 1-4 which states:

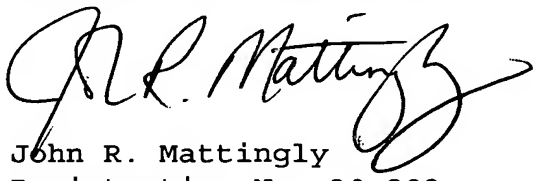
> "The access priority judgment unit 40 permits parallel access through the first and second access ports PT1 and PT2 when access through the first access port PT1 and access through the second access port PT2 use different DRAM macro structures."

Thus the claimed invention of claims 25-27, as amended, is not disclosed or suggested by Wu, and therefore the 35 USC 102(e) rejection should be withdrawn.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination is requested.

Respectfully submitted,



John R. Mattingly
Registration No. 30,293
Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: August 19, 2004